

FIGURE 1

09493031 012600

24

FIG. 2

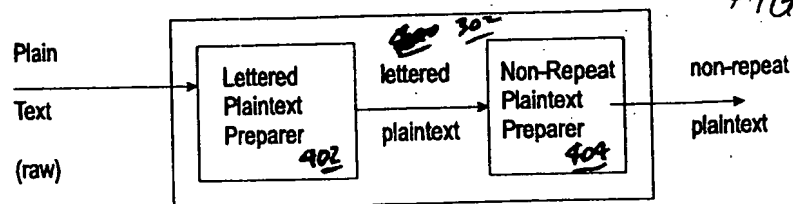


FIG. 5

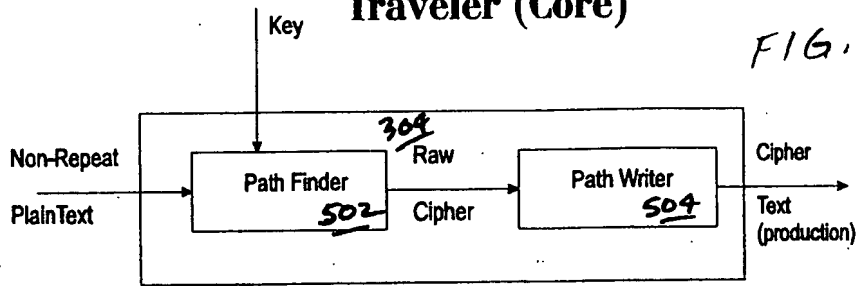
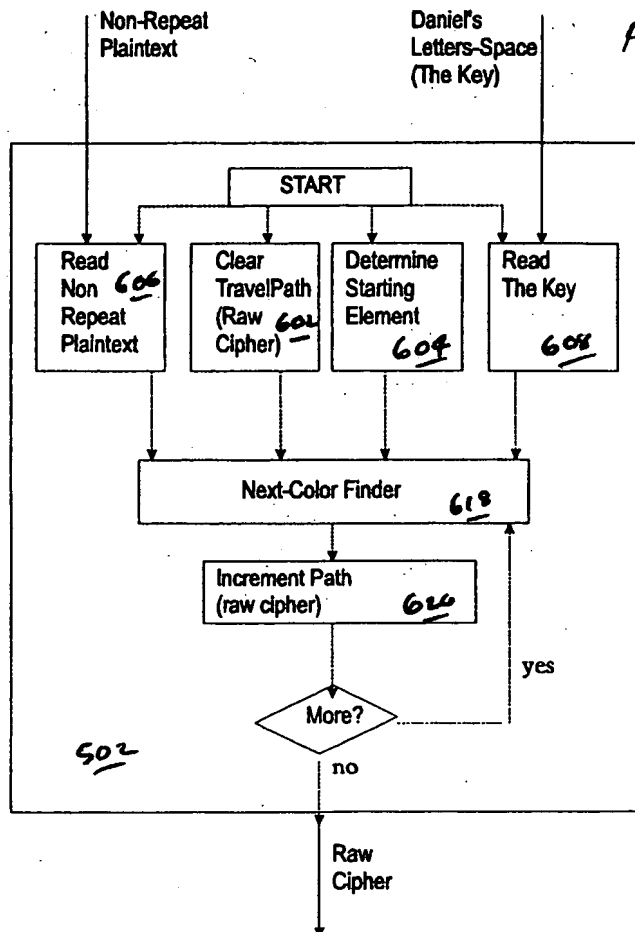


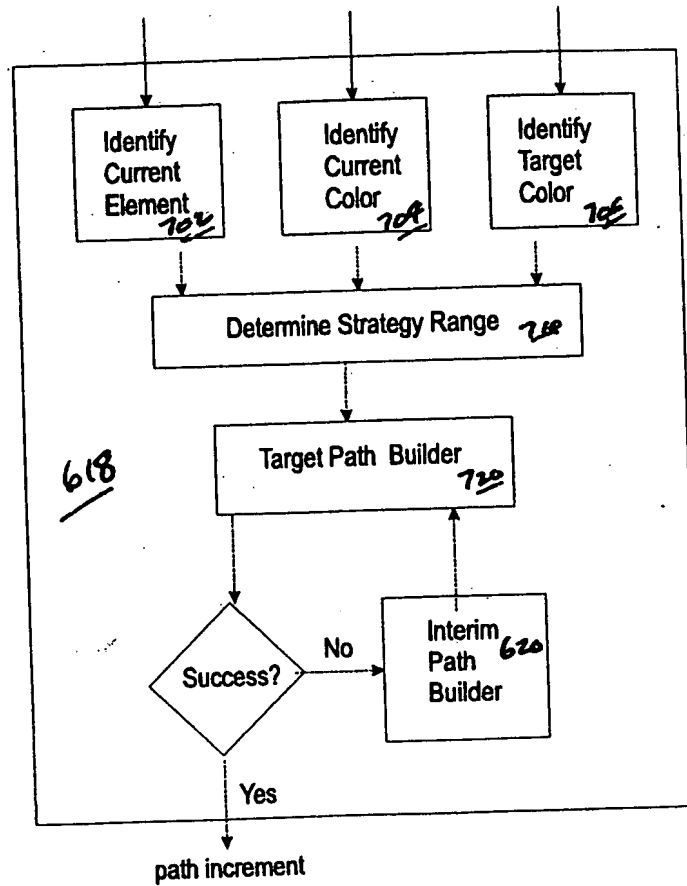
FIG. 6



2025年12月

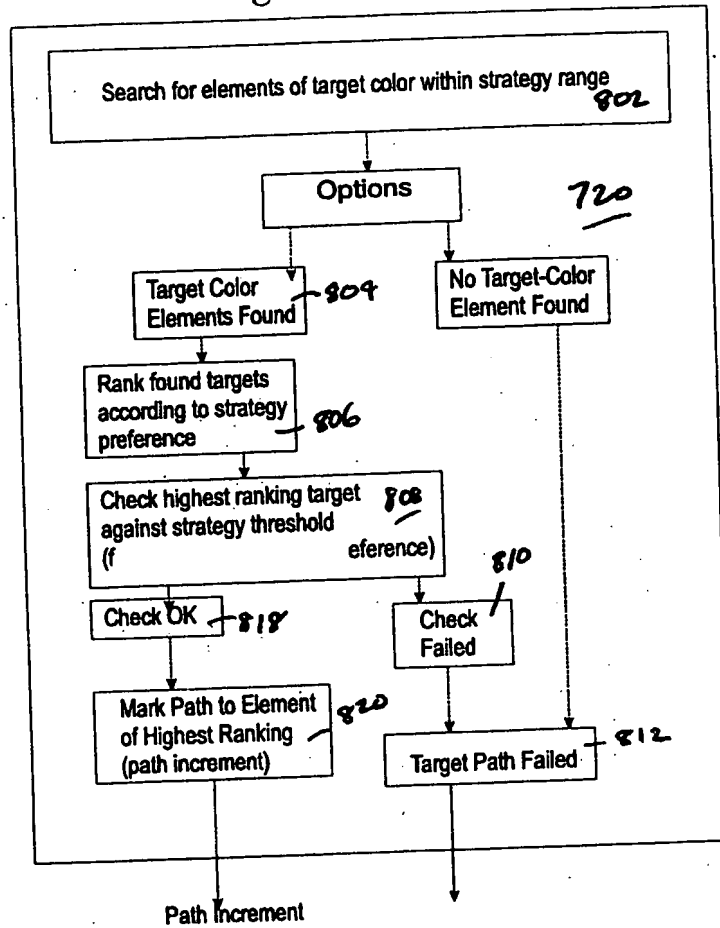
09-06-2017





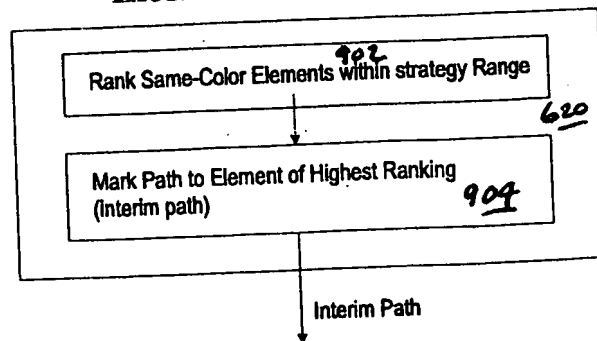
Target Path Builder

FIG. 8



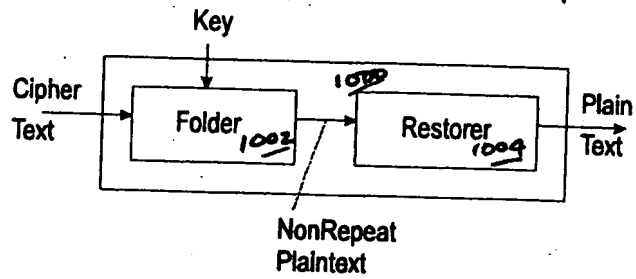
Interim Path Builder

FIG. 9



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Daniel Decryption *FIG. 10*



The Folder (Core)

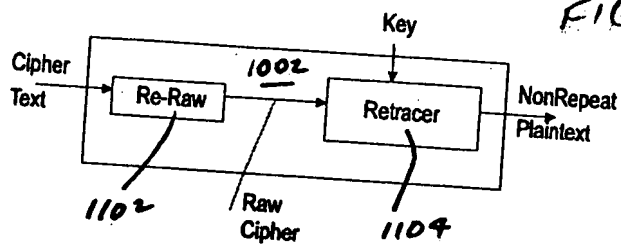


FIG. 12

FIG. 13



FIG. 14



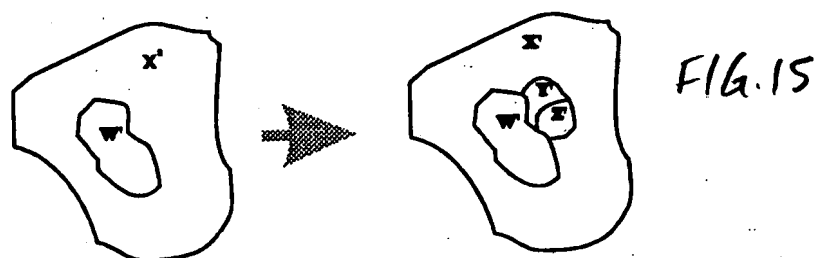
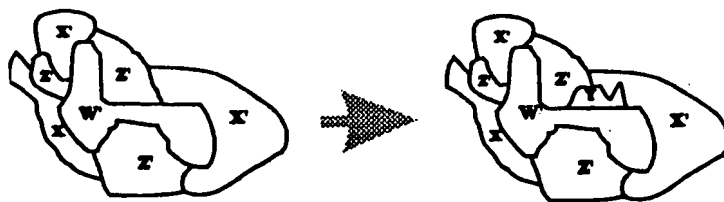
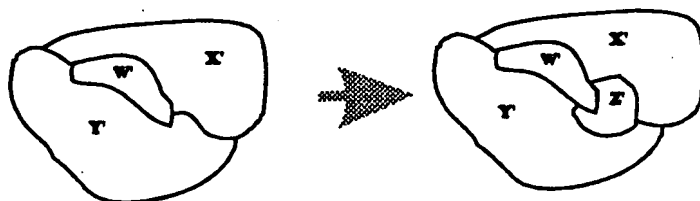
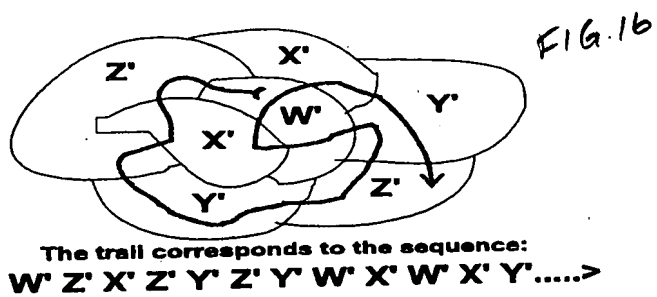


FIG. 15





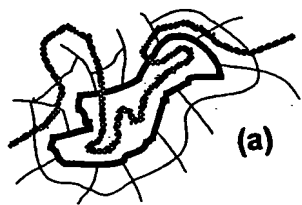


FIG 19 (a)

fig-5

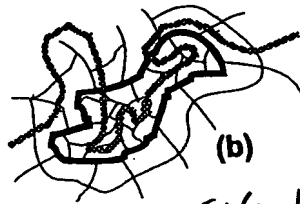
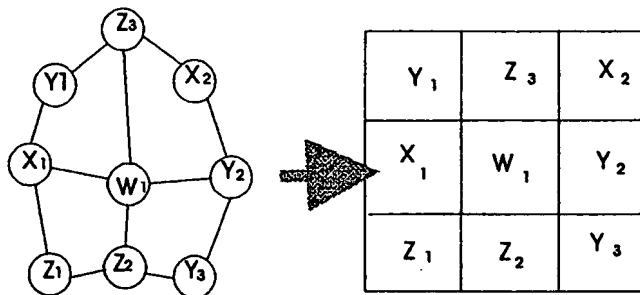


FIG. 19(b)



Equivalence between arc-represented graph and adjacency representation.

FIG. 20

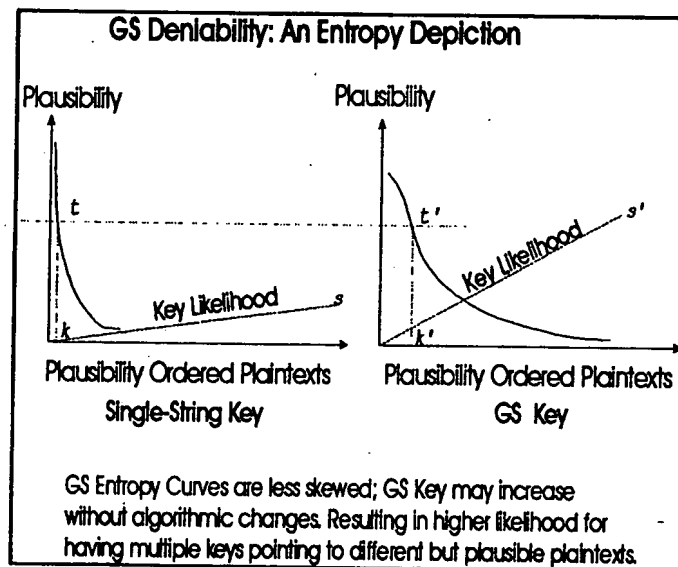


FIG. 21

The diagram illustrates a two-stage pipeline. The first stage is a block labeled 'gse' with input $m = g_1$ and control input $K1$. Its output is $c_1 = s$. The second stage is a block labeled 'gsr' with input $c_1 = s$ and control input $K2$. Its output is $c_2 = g_2$. Below the pipeline, a graph shows 'Text Size' on the y-axis and time on the x-axis. The text size is low during the initial phase, rises to a higher level during the interval labeled $g1 \rightarrow s$, and then falls back to the low level during the interval labeled $s \rightarrow g2$.

FIG. 22

Abstract

